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OMNIBUS Description and Specification

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http://www.innovative-dsp.com

This note is intended for users who wish to design Omnibus Modules.

This document details the OMNIBUS standard, including signal definitions, mechanical specifications and host processor board addressing and compatibility issues. Information on designing custom OMNIBUS module hardware is also included for those users who have specific interfacing needs not covered by the existing line of OMNIBUS modules.

Please note that this document discusses interfacing specifications for Innovative's line of TI DSP based OMNIBUS host cards. It is intended for use by designers wishing to implemented custom OMNIBUS module hardware for use with the M44, cM44, M6x, cM6x, SBC6x, and SBC6711 cards. While the ChicoPlus and Hombre cards are also OMNIBUS compatible, Innovative does not document the software support required to implement a custom OMNIBUS module on those host cards. Users wishing to custom design modules for use with ChicoPlus and Hombre should contact Innovative for more information.

Introduction

OMNIBUS is a modular mezzanine bus standard which allows a host processor board to accept plug-in modules which in turn implement hardware interfaces to external equipment. Modules may be memory mapped into host memory an all host cards, while certain host cards additionally provide alternative access methods (see below for details).

OMNIBUS is implemented as a 4.6" by 2" mezzanine board which uses two 50 pin high density connectors (called the "bus connectors") to implement the bus connections to the host hardware and an additional connector (called the "I/O connector") for use as a pass-through to connect to external hardware. The bus connector pinout is standard and allows the modules access to the host data bus, address bus, bus control lines (such as clock and

wait state control), timebase signals, processor interrupts, and power. The I/O connector pinout is unspecified and all fifty pins are available for use in connecting to external equipment. The block diagram below describes the connector arrangement.

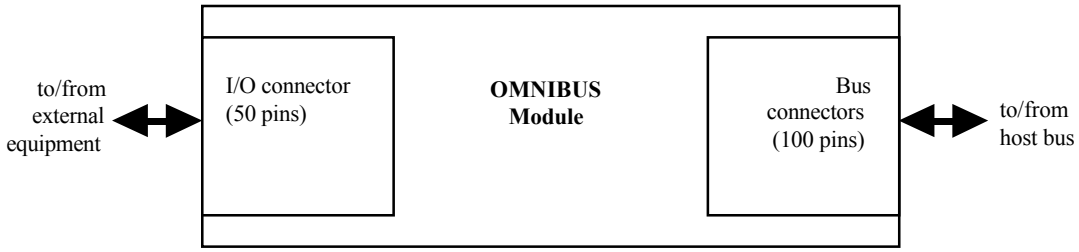

FIGURE 1. OMNIBUS Module Connector Block Diagram

Hosts can provide as many OMNIBUS slots as is mechanically and electrically possible given the host card's physical size, memory map, and power supply capabilities. Most Innovative hosts provide two slots (M44, cM44, M6x, SBC6x, SBC6711) while others provide three slots (cM6x).

Logical Specification

This section discusses the logical protocols and definitions of OMNIBUS accesses. Bus cycle format, handshaking, and memory mapping are discussed.

CYCLE DEFINITIONS

OMNIBUS is a synchronous parallel bus structure utilized multiple decode (chip select) signals per site, with subaddressing available for module-specific mapping of hardware to areas within each decode region. Hardware wait stating is implemented to allow the module to define the termination of each access. Modules may drive multiple independent interrupt signals back to the host. Numerous timing, power, and handshaking signals are also provided for support of module hardware and communications.

The following diagram gives the functional timing for module read and write accesses, and shows the relationship between the various bus control, address, and data signals.

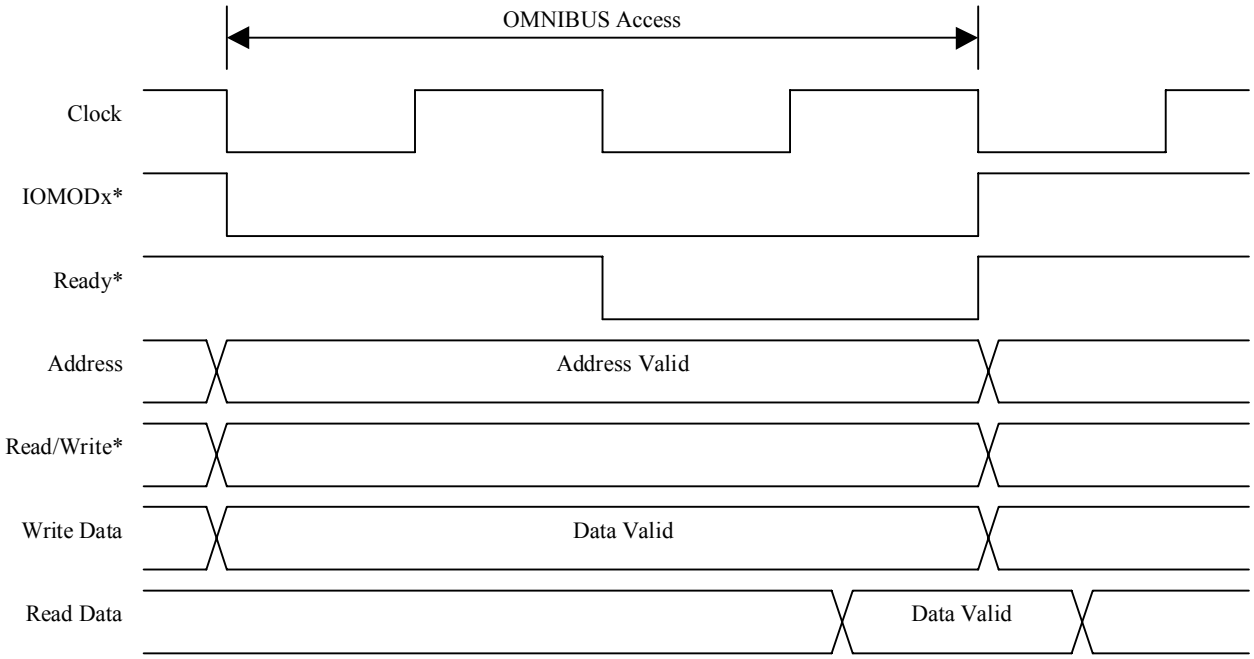

FIGURE 2. Functional Timing Diagram

OMNIBUS accesses are synchronous to a single clock, and start and stop on the falling edges of that clock. Accesses are defined by activity on the IOMODx* decoded chip select signals. An access is active when one of the IOMODx* signals is low. The bus is completely inactive when all IOMODx* signals to all available OMNIBUS sites on the host are high.

The minimum bus access length is two clocks, and there is a one clock dwell time between accesses which is required to define the accesses using IOMODx* low. This means that the maximum overall throughput on OMNIBUS is defined by a three clock cycle long period made up of the two cycle long IOMODx* pulse and one cycle of dwell time (IOMODx* high).

Bus access length is defined by ready signal generation from the module to the host. After the host asserts an IOMODx* signal low to indicate the beginning of an access, the OMNIBUS control logic on the host begins checking the hardware ready line from the module being accessed. The cycle will continue as long as the ready line is held high by the module. When the module wishes to terminate the cycle, it asserts the ready line low for one OMNIBUS clock cycle. This signals the host to bring IOMODx* high and terminate the cycle. In the case of a read access, data is latched into host hardware during the active low period of the ready cycle.

MEMORY MAPPING

OMNIBUS uses memory mapped accesses from the host board to exchange information with OMNIBUS modules. Four decoded active low module selects (IOMODx*) are provided per module slot, which may are further decodable via the twelve address pins on the bus connectors. The module selects go active low through the host's read or write access into a particular decoded memory region.

The exact location of each module site within the memory map of the host processor, as well as the amount of memory indicated by each module select, differs from host to host: see the individual host board's documentation for OMNIBUS memory map details.

Please note that the addressing used on the host boards to access the OMNIBUS mapped space varies from host to host. Specifically, 'C6x01 and 'C6711 boards used byte addressing while 'C44 boards use word (x32) addressing. This results in an address shift when accessing modules from an M44 as opposed to accessing them from an M67, for example.

For example, the description of the DIG module notes that the byte 3 direction control register for a module installed in site 0 is mapped to address IOMOD2 + 3. This address should be literally interpreted as 0x156000C on an M67, where IOMOD2 is equal to 0x1560000 and the offset adds decimal 12 (three 32-bit words of offset). IOMOD2 + 3 should be interpreted as 0x1560003 on an M44.

This addressing is most easily handled in C by using integer pointers and integer pointer arithmetic, which will always result in the required address alignment. For example, the following code defines a pointer and accesses the byte 3 direction control register with the documented offset:

```
unsigned int *pointer = 0x1560000;

*(pointer + 3) = 0x0;        /* set byte 3 to output mode */
```

The actual accessed memory location is 0x156000C, due to the way pointer math is handled in C.

INTERRUPTS

Each OMNIBUS site includes two active low edge sensitive interrupt signal pins on the bus connectors which allow modules to inform the host processor of events or conditions on the module. These lines are typically used to signal timing events or request data movement or processing from the host.

The interrupt signals are asynchronous with respect to the rest of the OMNIBUS signals. Interrupts should remain asserted until the required response is received from the host processor. In some cases (such as FIFO level interrupts) special handling may be required to avoid tripping multiple interrupts to the host. See the Design Tips section for more information.

Interrupt handling on the host boards varies by the host board used. See the host boards' documentation for details on how the interrupt signals can be detected and processed.

HOST-SPECIFIC COMMUNICATION FEATURES

Certain implementations of OMNIBUS include communications features not available on all host cards. These additional communications schemes allow for different methods of interfacing to module hardware and may be used in designs intended for specific hosts.

'C6x01/'C6711 McBSP Connections

Hosts based on the 'C6x01 and 'C6711 processors have the processors' McBSP ports connected to the OMNIBUS sites. This allows for serial data communication between module hardware and the host processor independent of the memory mapped bus interface.

See the host board's documentation for details on the McBSP connections to the board's OMNBUS sites, including expanding pinout information.

'C44 Comm Port Connections

The M44 and cM44 designs include comm port connections from the processor to each OMNIBUS module site. This allows modules to communicate with the host processor independently of the memory interface.

See the host board's documentation for details on the McBSP connections to the board's OMNBUS sites, including expanding pinout information.

Electrical Specification

BUS CONNECTOR PINOUTS

The OMNIBUS bus connectors (AMP P/N 173279-3 or equivalent) provide access to the hosts processor's bus for purposes of communication with the host. Present on the bus connectors are the data, address, bus control, timing, and power signals necessary to interact with the host processor. The two 50 pin bus connectors are nominally named "Bus Connector A" and "Bus Connector B" and each carries a subset of the signals.

The following tables gives the pinouts for the bus connectors.

Pin Number	Pin Name	Function	Direction (from host)
1, 19	DVCC	Digital +5V	O, Power
2, 20	DGND	Digital Ground	O, Power
3-18	D0-D15	Data bus 0-15	I/O
21, 43, 40, 45, 39, 26, 27	A0-A6	Address bus 0-6	O
28	RST*	Reset (active low)	O
29	INT0*	External Interrupt	I
30	RDY*	Bus ready (active low)	I (open-collector)
31	CLK	Clock	O
32	TMR0	Timer Channel	O
33	R/W	Read/Write	O
34	DDS	9850 Timebase	O
35-38	IOMODX*	OMNIBUS decoded selects (active low)	O
25	-12V	-12V	O, Power
23	+12V	+12V	O, Power
41, 42	AGND	Analog Ground	O, Power
22, 24	-15V	Analog -15V	O, Power
44, 46	+15V	Analog +15V	O, Power
47, 49	+5V	Analog +5V	O, Power
48, 50	-5V	Analog -5V	O, Power

TABLE 1. Bus Connector A Pinout

Pin Number	Pin Name	Function	Direction (from host)
1, 3-6	A7-A11	Address Bus 7-11	O
2, 19, 20, 49, 50	DGND	Digital Ground	O, Power
7-18	-------	Reserved	N/A
21	TMR1	Timer Channel	O
22	EXT TRIGx*	External Trigger	O
23, 25	+12V	+12V	O, Power
24	-------	Reserved	N/A
26	-------	Reserved	N/A
27	-------	Reserved	N/A
28	-------	Reserved	N/A
29	INT1*	External Interrupt	I
30	-------	Reserved	N/A
31	-------	Reserved	N/A
32	-------	Reserved	N/A
33-48	D16-D31	Data Bus 16-31	I/O

TABLE 2. Bus Connector B Pinout

Certain signals on the OMNIBUS connectors are dependent on support features which may vary from host to host. The DDS, timer, and interrupt signals are handled differently by each host. See the documentation for the host board for details on using these signals.

In addition to the standard signal set, most host cards provide additional processor-specific interface signals on bus connector B which can be used on modules designed specifically for those host cards. See the individual host card's documentation for details on the specific implementation used on a particular card.

SLOT TO SLOT PINOUT AND SIGNAL CONNECTION DIFFERENCES

Designers should note that certain signals vary by host board and OMNIBUS slot number. For example, the IOMODx signals are unique for each slot on a particular host. On all host cards, IOMOD0*, IOMOD1*, IOMOD2*, and IOMOD3* are connected to OMNIBUS slot zero, while IOMOD4*, IOMOD5*, IOMOD6*, and IOMOD7* are connected to slot one. In the case of the cM6x, signals IOMOD8*, IOMOD9*, IOMOD10*, and IOMOD11* are connected to site two. It is important to remember that these signal differences do not impact the design of an OMNIBUS module: they only change the memory region in which the module installed in a particular slot will respond. The same module design can be used in all slots on a particular host card, and the only thing that needs to be changed is the base IOMODx* addresses at which the software accesses the module.

Similarly, the external interrupt signals are connected differently on one OMNIBUS slot versus another at the host level. Each slot's interrupt signal connections on the host board are independent, but require either software changes or changes to jumper header configurations to connect the signals from the slots to the host board processor.

I/O CONNECTOR PINOUTS

The I/O connector (AMP P/N 173279-3 or equivalent) provides 50 pins of unspecified connectivity to a(n) external connector(s) on the host board which allow(s) external cabling to be connected to circuitry on the OMNIBUS module. These signals are specific to the particular module in use, and the types of external connectors present on the host board are par-

ticular to the host board in use (see the individual host card's Hardware Manual for details on the types of connectors used to make connections to the OMNIBUS I/O pins).

DC SPECIFICATIONS

Power Supplies

The OMNIBUS interface provides five separate power supplies for use by modules along with two separate ground return connections. The following table lists the supplies and their power ratings. A separate digital 5V supply is provided along with separate digital grounds to minimize the digital noise present on the analog power supplies.

Pin Name	Voltage	Current Rating (max)
DVCC	5V (digital)	(Host system dependent)
+12V	12V	(Host system dependent)
-12V	-12V	(Host system dependent)
+5V	5V (analog)	500 mA
-5V	-5V	500 mA
+15V	+15V	330 mA
-15V	-15V	330mA

TABLE 3. OMNIBUS Power Ratings

Please note that the AGND and DGND busses are separated on OMNIBUS host cards and for proper ground referencing they must be tied together on modules which use the analog power supplies (any supply other than digital 5V, 12V, or -12V). Innovative Integration recommends on module designs which use the analog supplies that separate ground planes (or copper pours on one plane) be used to create the two ground buses in order to prevent high frequency digital noise on the DGND bus from polluting the clean AGND return. The separate ground planes should be connected by a single trace (typically 0.050") or vias near the OMNIBUS bus connectors. This keeps high digital ground currents from flowing under sensitive analog componentry.

Signal Levels

OMNIBUS implements 5V tolerant TTL compatible signaling. The minimum defined output voltage is 2.4V high, 0.8V low for input and output from all OMNIBUS hosts. Signal outputs from a host card can swing on the high side up to 5V, so custom OMNIBUS module designs must be 5V tolerant. 3.3V based host cards (such as the M6x) are designed for 5V tolerance on the OMNIBUS connectors, so custom modules may use the digital 5V OMNIBUS power supply to power OMNIBUS pin drivers.

OMNIBUS does not provide a 3.3V supply: custom designs which require 3.3V (or other power supply voltage levels) must generate these supplies on the module from the existing 5V or 12V supplies. Innovative does not recommend using the +/-15V supplies for power generation except in low current requirement cases.

AC SPECIFICATIONS

The following diagrams give timing information for the OMNIBUS interface for the DSP based host boards. Separate timing diagrams are given for the 'C6x01 hosts, the M44, and the SBC6711. This data is derived from device design and component specifications and is not factory tested.

Timing information given below assumes the use of the factory default configuration data for external bus control for the processors used on each type of host. Using values other than the recommended ones may alter the timing of the OMNI-BUS signals on the host.

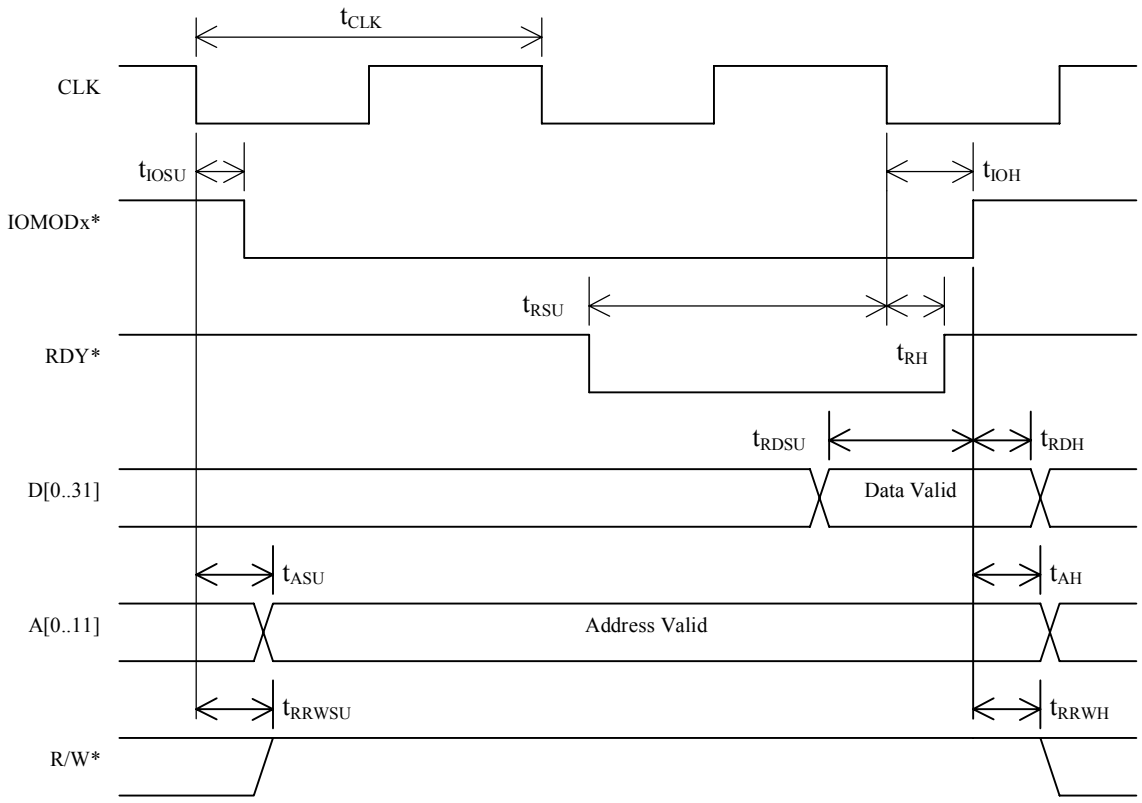

FIGURE 3. M6x/cM6x/SBC6x OMNIBUS Read Cycle Timing

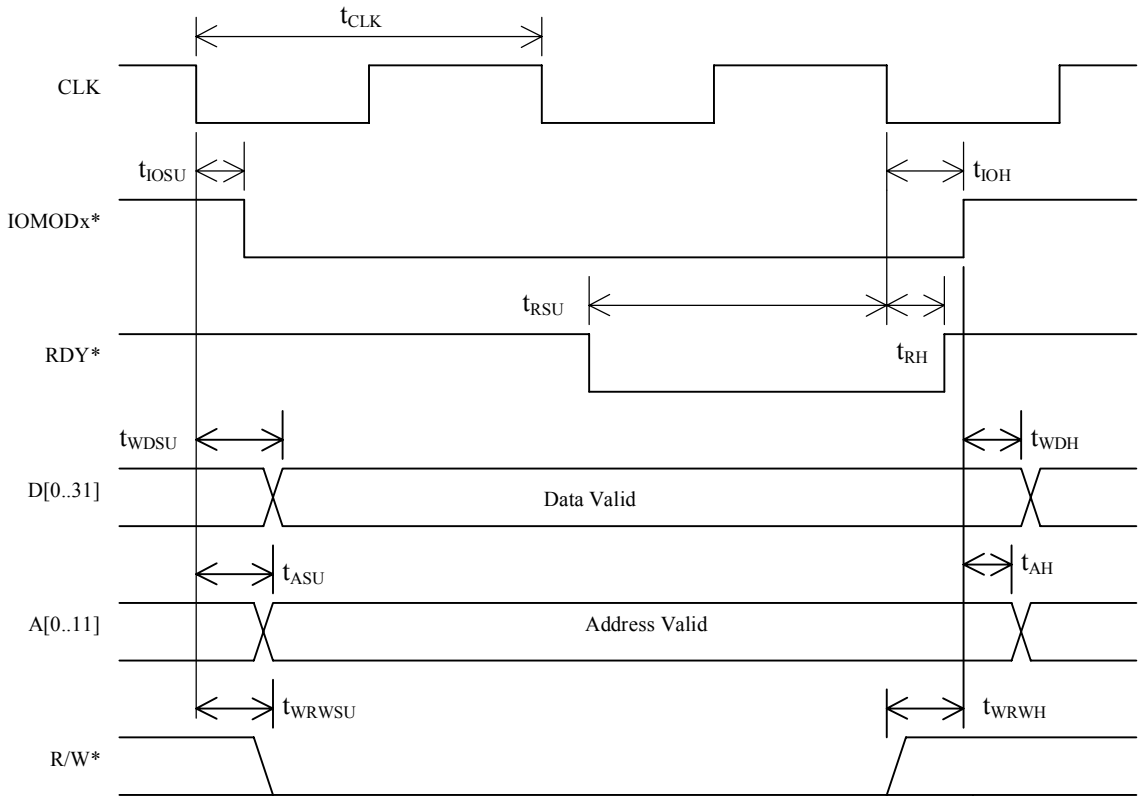

FIGURE 4. M6x/cM6x/SBC6x OMNIBUS Write Cycle Timing

Parameter	min. (ns)	max. (ns)
t_{CLK}	40	
t_{IOSU}	-5	5
t_{IOH}(see text)	N/A	N/A
t_{RSU}	20	
t_{RH}	0	
t_{RDSU}	12	
t_{RDH}	0	
t_{WDSU}	See text	0
t_{WDH}	15	
t_{ASU}	See text	0
t_{AH}	0	
t_{RRWSU}		0
t_{RRWH}	0	
t_{WRWSU}	See text	0
t_{WRWH}		17

TABLE 4. M6x/cM6x/SBC6x OMNIBUS Cycle Timing Parameters

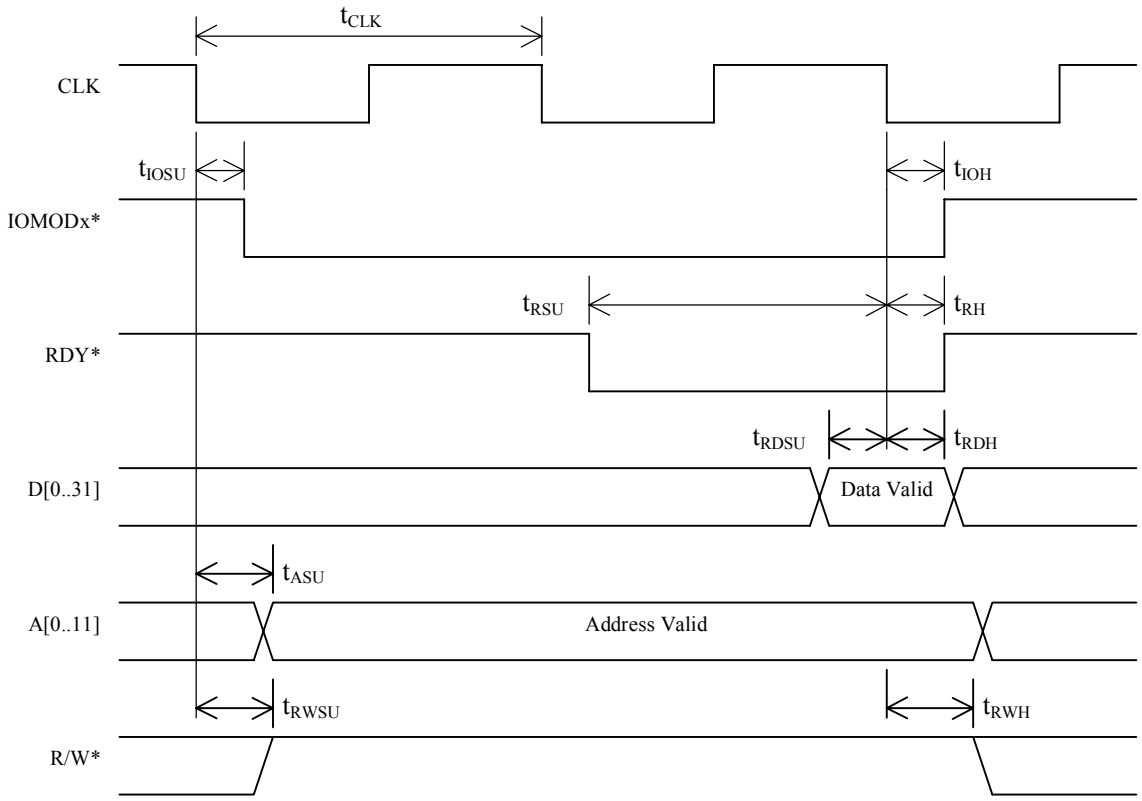

FIGURE 5. M44/cM44 OMNIBUS Read Cycle Timing

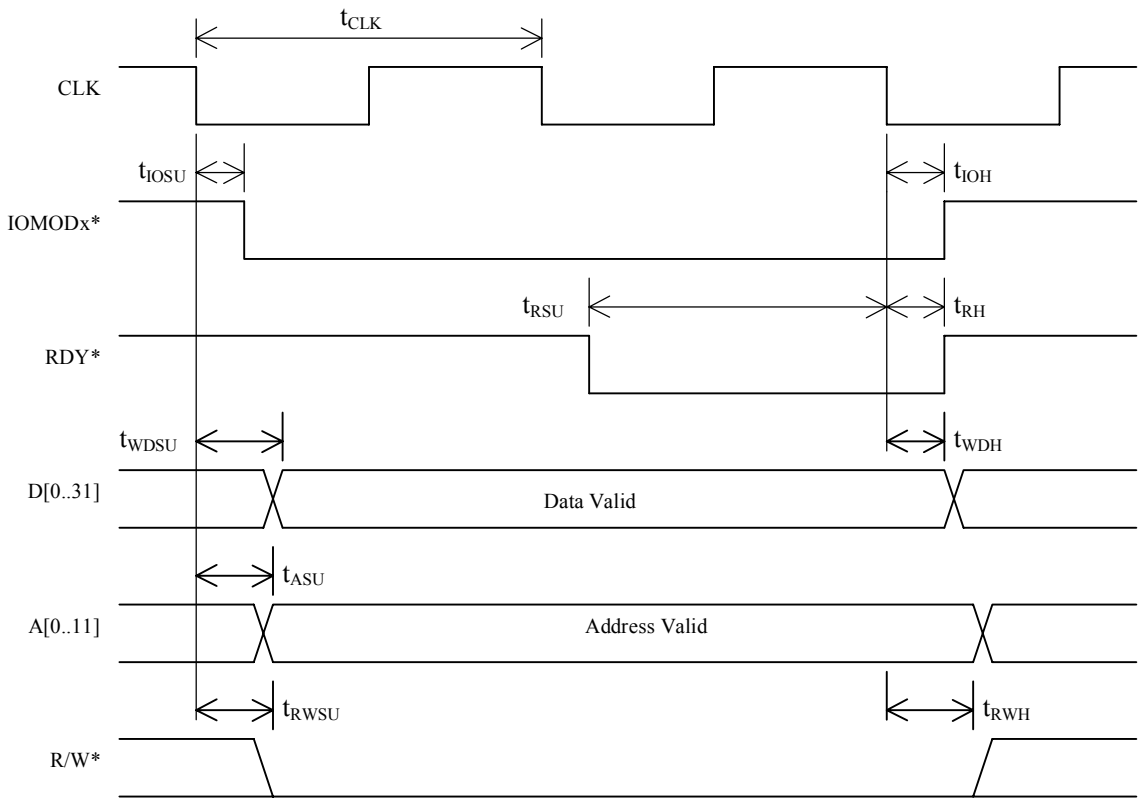

FIGURE 6. M44/cM44 OMNIBUS Write Cycle Timing

Parameter	min. (ns)	max. (ns)
t_{CLK}	33	50
t_{IOSU}	0	15
t_{IOH}	0	15
t_{RSU}	20	
t_{RH}	0	
t_{RDSU}	10	
t_{RDH}	0	
t_{WDSU}		16
t_{WDH}	15	
t_{ASU}		9
t_{RWSU}		9
t_{RWH}		9

TABLE 5. M44/cM44 OMNIBUS Read Cycle Timing Parameters

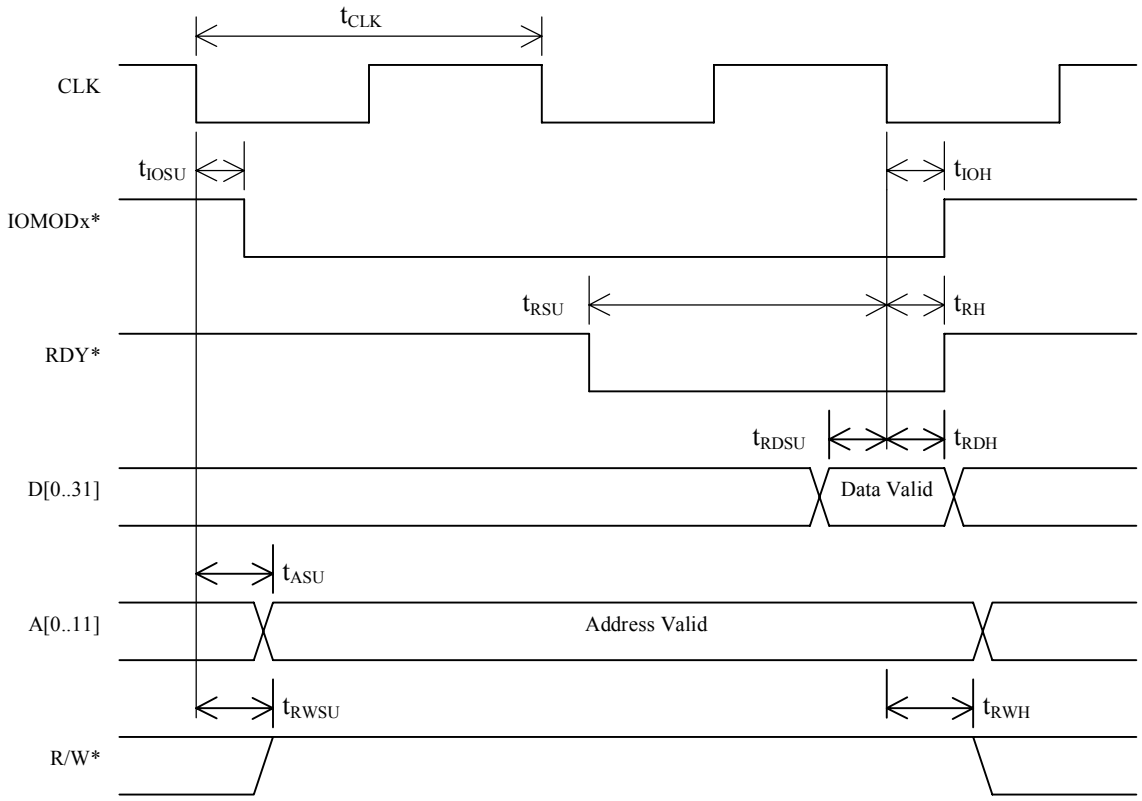

FIGURE 7. SBC6711 OMNIBUS Read Cycle Timing

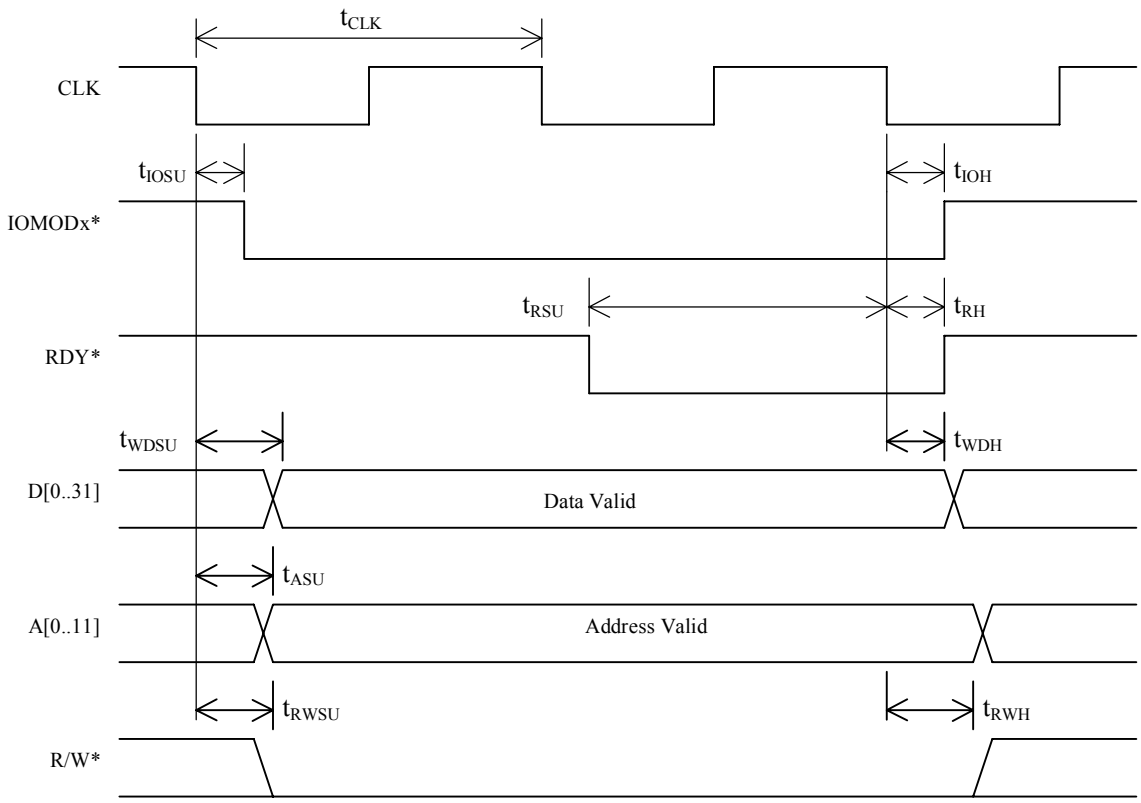

FIGURE 8. SBC6711 OMNIBUS Write Cycle Timing

Parameter	min. (ns)	max. (ns)
t_{CLK}	26	
t_{IOSU}		5
t_{IOH}		5
t_{RSU}	26	
t_{RH}	0	
t_{RDSU}	35	
t_{RDH}	0	
t_{WDSU}		0
t_{WDH}	0	
t_{ASU}		0
t_{AH}	0	
t_{RWSU}		0
t_{RWH}	0	

TABLE 6. SBC6711 OMNIBUS Cycle Timing Parameters

Additional Timing Notes

'C6x01 host cards implement OMNIBUS as a retimed slower speed version of the processor's external memory interface. Since the processor bus interface runs at several times the nominal speed of the classic OMNIBUS specification, glue logic is used to retime the various bus control signals generated by the 'C6x01 to more closely match OMNIBUS standard timings.

A side effect of the clock rate translation is that 'C6x01 external bus accesses do not start and stop on OMNIBUS clock cycle edges. The host board interface logic retimes the leading edge of each access to create an OMNIBUS IOMODx* pulse whose leading edge is compatible with OMNIBUS standard timing, but the trailing edge of the IOMODx* signal must follow the processor access. The net effect is that while the leading edges of IOMODx* pulses will always be synchronized to the OMNIBUS clock, the trailing edges will vary in phase with respect to the OMNIBUS clock from access to access. The phase of the trailing edge of the IOMODx* pulse is not predictable, so module logic designed to respond to the access must not assume a relationship between the IOMODx* trailing edge and the OMNIBUS clock.

Please also note that the R/W* signal for 'C6x01 hosts is not active through the entire IOMODx* strobe period and so should be sampled for use at the beginning of each access.

This document provides recommendations for logic design which include consideration of the above characteristics. Please see the Design Tips section for more information.

Signal Termination

Innovative recommends the use of series termination resistors in each bus signal connected on an OMNIBUS module. The recommended value is 33 ohms, but this value may need to be adjusted depending on signal loading and routing on the module design. Signal quality should be carefully checked for over- and undershoot at the destination. Other termination arrangements, such as pullup/down AC terminators, may be used if desired.

Innovative does not publish IBIS or SPICE simulation models of its host boards.

Mechanical Specification

OMNIBUS uses a mezzanine (sandwich) board design which allows modules to electrically and mechanically connect to the host card with the module lying in a parallel plane to that of the host. Modules are held in place by three 50 pin connectors and may optionally be secured to the host via screws and standoffs at the connector ends.

MECHANICAL DEFINITIONS

Included in the OMNIBUS specification package are mechanical drawings for the host and module board designs.

MOD_DIM.PDF gives the dimensions for module PCB size and connector location, as well as the pin orientation of the connectors. When laying out the OMNIBUS module PCB, refer to the connector data sheet for complete pin numbering information.

HOST_DIM.PDF gives the vertical spacing of seated OMNIBUS modules on host cards, as well as the intersite spacing on the host cards. This information is useful in defining component height clearances from both sides of the OMNIBUS module, as well as connector positioning for double-wide OMNIBUS module designs (i.e. modules which span two OMNIBUS sites and connect to connectors on both sites).

MODULE.DXF gives a DXF format version of the board outline and connector positioning of an OMNIBUS module. This provides machine-readable mechanical information which allows the user to skip the step of drawing and positioning the board outline and connectors.

Module Design Guidelines

The following information includes tips and reference design material for use in creating a custom OMNIBUS design. The recommendations are divided into sections dealing with the logical, electrical, and mechanical aspects of the specification.

LOGICAL DESIGN

In creating custom logic or discrete semiconductor designs, it is recommended that the user filter glitch sensitive signals such as reset. Modern high-speed logic is necessarily sensitive to fast edges and small, fast glitches on signals such as reset can cause difficult to diagnose failures. If reset is handled entirely in programmable logic, a digital filter can be used to detect and trigger on reset signals which are active for several OMNIBUS clocks, rather than directly connecting the OMNIBUS reset to the required logic. If reset must be observed by discrete logic or other circuitry, an RC filter and/or careful termination is required to ensure glitch and noise immunity.

Use care when detecting and responding to OMNIBUS accesses on 'C6x01 hosts, as these cards do not have predictable rising-edge IOMODx and R/W timing with respect to the OMNIBUS clock. Accesses should be detected at the falling edge of IOMODx and their state latched so that the appropriate response can be generated through the end of the IOMODx active region.

Wherever possible, module designs should provide real-time buffering for data which cannot be lost if the host card is unable to service the module within a timely fashion. Many sources of temporary data transfer bottlenecks exist which can cause the host to be busy for time periods which could cause data gaps in I/O streams processed by the OMNIBUS module. For example, if the host is busy servicing another interrupt (say from PCI bus I/O or a USB port) it may not be able to get to the module's requirements in time to transfer time critical data. If this is the case, data may be lost causing potential system problems. If buffering is provided in hardware for such time critical data, instantaneous gaps in host processing will not cause data loss. Such buffering is typically implemented via a hardware memory element such as a FIFO or dual ported memory.

An example logic design, written in the VHDL language, is included to illustrate good design practices for OMNIBUS glue logic.

Example Glue Logic Design

state, register logic, and FIFO control logic which will be interfaced to OMNIBUS. Created under the Xilinx toolset but portable to other vendors' HDL logic design tools, OMNIBUS.VHD can be used as the basis for a VHDL coded OMNIBUS interface logic design.

OMNIBUS.VHD implements an OMNIBUS interface to independent read and write FIFOs as well as an example control register. The design uses access detection logic to trigger read and write accesses to the FIFO memories and control the advancement of the FIFO pointers.

The FIFO system is based on Xilinx COREGEN asynchronous FIFO cores. These cores implement two independent unidirectional buffer memories. One FIFO receives data from external hardware and buffers it for use by the OMNBIBUS host, while the other receives data from the OMNIBUS host and buffers it for use by external hardware. This type of memory buffer architecture is used in most systems which require rate matching between two different clock domains (i.e. data is generated by one system at one clock rate and processed by another system at a different clock rate). The external interface is driven by clock and write/read enable signals which are independent from each other and also independent from the OMNIBUS clock and access rate.

While this example instantiates FIFO buffers internal to the programmable logic device itself, OMNIBUS designs can of course support the use of stand-alone FIFOs (from manufacturers like Cypress Semiconductor, IDT, and Texas Instruments). In this case appropriate control logic would generate the handshaking signals necessary to communicate with the standalone FIFOs. The user is cautioned, however, to pay close attention to the loading on the OMNIBUS data signals, as heavy loads generated by multiple FIFOs can cause termination and drive problems.

ELECTRICAL DESIGN

Minimize bus loading, ideally using only one load per OMNIBUS pin. If several logic loads are required to connect to a single OMNIBUS signal, buffer the signal through FCT/ABT logic or through programmable logic.

Close attention should be paid to termination and quality of applicable OMNIBUS signals. Termination resistors are recommended (see above), and may need to be tuned for the particular application and loading.

An example schematic giving connector pinouts for the OMNIBUS bus connectors is included as part of the specification package. The schematic is compatible with the OrCAD Capture schematic package, and may be found in the files OMNI_EX.DSN and OMNI_EX.OPJ.

MECHANICAL DESIGN

Please refer to the mechanical drawings given in the design package for details on dimension of the OMNIBUS specification.

OMNIBUS PCB designs should take care to observe the limits specified by the mechanical drawings. To ensure compatibility with Innovative's host cards, do not exceed the basic module PCB dimensions given in this specification. Innovative's host designs take care to comply with the height specification given within the module PCB dimensions, but host boards may have significantly taller components outside the specified module PCB space. Exceeding the PCB dimensions in a custom module design may cause a mechanical conflict with components on current or future host boards.

To comply with the PCI and cPCI specifications for single slot component height, module designs must follow the maximum component height specifications given in the mechanical drawings. Exceeding the maximum component height off of the top of the module may place the module/host assembly in conflict with hardware installed in neighboring slots in PCI/cPCI systems.

In most cases the OMNIBUS connector mating force will be sufficient to mechanically capture the module to the host board. Systems which require positive mechanical retention of the module to the host can use screws and standoffs matched to the OMNIBUS connectors. See the connector data sheets for manufacturer's recommendations on mounting hardware.